

In the Claims:

1. (Currently Amended) A multi-layer semiconductor wafer structure defining a multiplicity of dies formed thereon, said wafer structure comprising:

a first scribe line having a selected width  $S_1$  extending along a first direction and defining a first edge of adjacent a first die of said multiplicity of dies;

a second scribe line having a selected width  $S_2$  extending along a second direction and defining a second edge of adjacent said first die and intersecting said first scribe line, and said first and second edges intersecting at a corner point of said first die;

~~at least one free~~ a first restricted area  $A_1$  defined on at least one of said first and second scribe line ~~[[lines]]~~ where placement of a test key is restricted, and said first restricted area  $A_1$  is defined by the equation  $A_1 = D_1 \times S_1$ , where  $D_1$  is the distance along the first edge extending from the corner point of the first die;

a second restricted area  $A_S$  at the intersection of said first scribe line and said second scribe line wherein said second restricted area  $A_S$  is defined by the equation  $A_S = S_1 \times S_2$ ;

at least one first test key formed on one of said first and second scribe lines, but not on said restricted areas A and  $A_S$ ; and

at least one second test key formed in at least one of said restricted areas A and  $A_S$ .

2. (Original) The multi-layer semiconductor wafer structure of claim 1 wherein at least one layer of said wafer structure is a low-k dielectric layer.

3. (Previously Presented) The multi-layer semiconductor wafer structure of claim 2 wherein the low-k dielectric layer has a dielectric constant of less than approximately 3.5.

4. (Original) The multi-layer semiconductor wafer structure of claim 3 wherein the low-k dielectric layer has a dielectric constant of less than 3.0.
5. (Previously Presented) The multi-layer semiconductor wafer structure of claim 2 wherein the low-k dielectric layer is a material selected from the group consisting of CVD-SiOC, SiOCN, Spin-on SiOC, CVD deposited polymer, Spin-on polymer, FSG, SiO<sub>2</sub> and combinations thereof.
6. (Canceled)
7. (Currently Amended) The multi-layer semiconductor wafer structure of claim 1 wherein the free areas are ~~area is~~ defined on the top layer of the multi-layer structure.
8. (Currently Amended) The multi-layer semiconductor wafer structure of claim 1 wherein the free areas are ~~area is~~ defined on at least one of the top three layers of the multi-layer structure.
9. (Currently Amended) The multi-layer semiconductor wafer structure of claim 1 wherein ~~said 6 further comprising~~ at least one second test key is formed in said first restricted ~~free~~ area, said at least one second test key having a measurement ratio  $R_1$ , wherein the measurement ratio is defined by the equation:  $R_1 = M_1/A_1$ , wherein  $M_1$  is the total area of said at least one second test key formed on the first restricted ~~free~~ area  $A_1$ , and  $R_1$  is less than about 10%.

10. (Currently Amended) The multi-layer semiconductor wafer structure of claim [[6]] 1 wherein the distance  $D_1$  is less than about  $600\mu\text{m}$ .

11. (Currently Amended) The multi-layer semiconductor wafer structure of claim [[6]] 1 wherein the width  $S_1$  of the first scribe line is greater than about  $20\mu\text{m}$ .

12. (Original) The multi-layer semiconductor wafer structure of claim 1 wherein the multi-layer structure is formed on a substrate selected from the group consisting of bulk Si, SOI, SiGe, GaAs, InP, and a combination thereof.

13. (Previously Presented) The multi-layer semiconductor wafer structure of claim 1 wherein said first die comprises:

a first peripheral region inside of and extending parallel to said first scribe line;

a second peripheral region inside of and extending parallel to said second scribe line and intersecting said first peripheral region to form a corner area;

a conductive ring formed between said first die and said first peripheral region and said second peripheral region; and

an array of apertures formed in the conductive ring and adjacent the corner area of the first die.

14. (Original) The multi-layer semiconductor wafer structure of claim 13 wherein said array of apertures comprises at least two slots.

15. (Original) The multi-layer semiconductor wafer structure of claim 13 wherein said array of apertures comprises two rows of holes.

16. (Original) The multi-layer semiconductor wafer structure of claim 13 wherein the array of apertures extends along at least one of the first peripheral region and the second peripheral region.

17. (Previously Presented) The multi-layer semiconductor wafer structure of claim 13 wherein the first die further comprises a circuit area with a plurality of circuit elements, wherein the conductive ring is electrically connected to the circuit elements to apply one of a power source and a ground potential to the circuit elements.

18. (Original) The multi-layer semiconductor wafer structure of claim 13 wherein the conductive ring has a width of between 50 $\mu$ m and about 300 $\mu$ m.

19. (Canceled)

20. (Currently Amended) The multi-layer semiconductor wafer structure of claim 1 wherein ~~said 19 further comprising~~ at least one second test key is formed on said second restricted free area  $A_S$ , said second test key having a measurement ratio  $R_S$  that is less than 10% and is defined by the equation  $R_S = M_S / A_S$ , wherein  $M_S$  is the total area of said at least one second test key formed on the second restricted free-area  $A_S$ .

21. (Currently Amended) The multi-layer semiconductor wafer structure of claim 1 [[19]] wherein the width of the scribe lines  $S_1$  and  $S_2$  is greater than about  $20\mu\text{m}$ .

22. (Currently Amended) The multi-layer semiconductor wafer structure of claim 1 wherein said at least one first restricted ~~free~~ area comprises a first free area  $A_1$  on the first scribe line and another first ~~a second~~ free area  $A_2$  on the second scribe line, ~~said first free area defined by the equation  $A_1 = D_1 \times S_1$  where  $D_1$  is the distance along the first direction extending from the corner point of the die and  $S_1$  is the width of the first scribe line, said second free area defined by the equation  $A_2 = D_2 \times S_2$  where  $D_2$  is the distance along the second edge direction extending from the corner point of the first die and  $S_2$  is the width of the second scribe line.~~

23. (Canceled)

24. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 [[23]] further comprising:

at least one test key formed on at least one of the free areas  $A_1$ ,  $A_2$  and  $A_S$ ;

wherein a first measurement ratio  $R_1$  is defined as the equation  $R_1 = M_1/A_1$ , wherein  $M_1$  is the total area of the test keys formed on the first free area  $A_1$ ;

wherein a second measurement ratio  $R_2$  is defined as the equation  $R_2 = M_2/A_2$ , wherein  $M_2$  is the total area of the test keys formed on the second free area  $A_2$ ;

wherein a third measurement ratio  $R_S$  is defined as the equation  $R_S = M_S/A_S$ , wherein  $M_S$  is the total area of the test keys formed on the third area  $A_S$ ; and

wherein a total measurement ratio R is defined as the equation  $R = (M_1 + M_2 + M_S) / (A_1 + A_2 + A_S)$ .

25. (Original) The multi-layer semiconductor wafer structure of claim 24 wherein  $R_1$  is less than about 10%.

26. (Original) The multi-layer semiconductor wafer structure of claim 24 wherein  $R_2$  is less than about 10%.

27. (Original) The multi-layer semiconductor wafer structure of claim 24 wherein  $R_S$  is less than about 10%.

28. (Original) The multi-layer semiconductor wafer structure of claim 24 wherein the ratio R is less than about 10%.

29. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 wherein the first distance  $D_1$  is less than about 600 $\mu\text{m}$ .

30. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 wherein the distance  $D_2$  along the second direction is less than about 600 $\mu\text{m}$ .

31. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 wherein the width  $S_1$  of the first scribe line is greater than about 20 $\mu\text{m}$ .

32. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 wherein the width  $S_2$  of the second scribe line is greater than about  $20\mu\text{m}$ .

33. (Original) A multi-layer semiconductor wafer structure defining a multiplicity of dies formed thereon, said wafer structure comprising:

a first scribe line having a selected width extending along a first direction;

a second scribe line having a selected width extending along a second direction and intersecting said first scribe line;

four dies located at and separated by the intersection of said first and second scribe lines wherein each of the four dies comprises a corner point adjacent the intersection of said first and second scribe lines;

a first free area  $A_1$  on the first scribe line adjacent the corner point of the first die, wherein  $A_1$  is defined by the equation  $A_1 = D_1 \times S_1$  and wherein  $D_1$  is the distance extending from the corner point of the first die, and  $S_1$  is the width of the first scribe line;

a second free area  $A_2$  on the second scribe line adjacent the corner point of the second die, wherein  $A_2$  is defined by the equation  $A_2 = D_2 \times S_2$ , and wherein  $D_2$  is the distance from the corner point of the second die, and  $S_2$  is the width of the second scribe line;

a third free area  $A_3$  on the second scribe line adjacent the third corner point of the third die, wherein  $A_3$  is defined by the equation  $A_3 = D_3 \times S_2$ , and wherein  $D_3$  is the distance from the corner point of the third die;

a fourth free area  $A_4$  on the first scribe line adjacent the corner point of the fourth die, wherein  $A_4$  is defined by the equation  $A_4 = D_4 \times S_1$ , and wherein  $D_4$  is the distance from the corner point of the fourth die; and

a fifth free area  $A_5$  on the intersection of the first scribe line and the second scribe line and is defined by the equation  $A_5=S_1 \times S_2$ .

34. (Original) The semiconductor wafer of claim 33 further comprising:

at least one test key formed on at least one of the free areas  $A_1$ ,  $A_2$ ,  $A_3$ ,  $A_4$  and  $A_5$ ;

wherein a first measurement ratio  $R_1$  is defined as the equation  $R_1=M_1/A_1$ , wherein  $M_1$  is the total area of the test keys formed on the first free area  $A_1$ ;

wherein a second measurement ratio  $R_2$  is defined as the equation:  $R_2= M_2/A_2$ , wherein  $M_2$  is the total area of the test keys formed on the second free area  $A_2$ ;

wherein a third measurement ratio  $R_3$  is defined as the equation:  $R_3= M_3/A_3$ , wherein  $M_3$  is the total area of the test keys formed on the third free area  $A_3$ ;

wherein a fourth measurement ratio  $R_4$  is defined as the equation:  $R_4= M_4/A_4$ , wherein  $M_4$  is the total area of the test keys formed on the fourth free area  $A_4$ ;

wherein a fifth measurement ratio  $R_5$  is defined as the equation:  $R_5= M_5/A_5$ , wherein  $M_5$  is the total area of the test keys formed on the fifth free area  $A_5$ ; and

wherein a total measurement ration  $R$  is defined as the equation  $R=(M_1+M_2+M_3+M_4+M_5) / (A_1+A_2+A_3+A_4+A_5)$ .

35. (Original) The semiconductor wafer of claim 34 wherein the first measurement ratio  $R_1$  is less than about 10%.

36. (Original) The semiconductor wafer of claim 33 wherein the distance  $D_4$  is less than about 600 $\mu$ m.



37. (Original) The semiconductor wafer of claim 33 wherein the width  $S_1$  of the first scribe line is greater than about 20 $\mu$ m.

38. (Original) The semiconductor wafer of claim 33 wherein the width  $S_2$  of the second scribe line is greater than about 20 $\mu$ m.

39. (Original) The semiconductor wafer of claim 33 wherein the multi-layer structure is formed on a substrate selected from the group consisting of bulk Si, SOI, SiGe, GaAs and InP.

40. (Original) The semiconductor wafer of claim 33 wherein each of said four dies comprises:

- a first peripheral region parallel to said first scribe line;
- a second peripheral region parallel to said second scribe line;
- a conductive ring formed between said die and said first peripheral region and said second peripheral region; and
- an array of apertures formed in the conductive ring and adjacent the corner area of the die.

41. (Previously Presented) The semiconductor wafer of claim 33 wherein at least one layer of the multilayered wafer structure is a low-k dielectric layer-having a dielectric constant less than approximately 3.5.

42. (Original) The semiconductor wafer of claim 40 wherein the array of apertures comprises two rows of holes.

43. (Original) The semiconductor wafer of claim 41 wherein said array of apertures comprises at least two slots.
44. (Original) The semiconductor wafer of claim 40 wherein the array of apertures extends along at least one of the first peripheral region and the second peripheral region.
45. (Original) The semiconductor wafer of claim 40, wherein each of the four dies further comprises a circuit area with a plurality of circuit elements, wherein the conductive ring is electrically connected to the circuit elements to apply one of a power source and a ground potential to the circuit elements.
46. (Original) The semiconductor wafer of claim 40 wherein the conductive ring has a width of between about 50 $\mu$ m and 300 $\mu$ m.
- 47.-64. (Canceled)
65. (New) The multilayer semiconductor wafer structure of claim 9 wherein at least another second test key is formed on said second restricted area  $A_S$ , said at least another second test key having a measurement ratio  $R_S$  that is less than 10%, said measurement ration  $R_S$  defined by the equation  $R_S=M_S/A_S$ , wherein  $M_S$  is the total area of said at least another second test key formed on said second restricted area  $A_S$ .